Christopher Avila

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OBJECTIVE

Current senior aspiring to add value to a mission driven company for the summer of 2025. Proficient in **Altium Designer, Cadence Virtuoso, Verilog, C/C++**, and **Python.** I am interested in Analog & Digital Design, Tests / Verification, VLSI, and Embedded Systems.

EDUCATION

Texas A&M University (TAMU), College Station, Texas
Bachelor of Science in Computer Engineering, ***May 2025***

RELEVANT COURSEWORK

Computer Architecture and Design, Electronics, Microprocessor Systems Design
Signals and Systems, Digital Integrated Circuit Design, Computer System Design

WORK EXPERIENCE

The Toro Company – Ditch Witch
Hardware / Software Engineer Intern, May 2024 – August 2024

- Developed **deep learning** techniques using **Caffe** and Holistically Nested Edge Detection, enhancing **autonomous** navigation capabilities.
- Created a **C++** program utilizing **OpenCV** to select detected lines
- Collaborated on **hardware proposals** for R&D, improving board performance
- Built a third-order low pass filter **PCB** to filter noise on a DC powerline

PROJECTS

LED Matrix Audio Visualizer – *C++ / Hardware*

- Programmed an **Arduino Nano** to control LED matrices, displaying real time frequency data using FFT (Fast Fourier Transform)
- Utilized **SPI communication** to interface with multiple 8x32 LED matrices
- Integrated 1602 **LCD** screen with **I2C communication** to display information
- Employed **bit-level manipulation** and mapping techniques to visualize frequency magnitudes

Intelligent Piano Notes Visualizer – *Python / Hardware*

- Designed and implemented a piano notes visualizer with a 1700-LED array using LED strips, a Raspberry Pi 4B, and an LCD screen.
- Developed Python scripts to control LED strips, enabling real time animations synchronized with MIDI input.
- Built hardware setup including wiring diagrams, LED matrix configuration, and system integration.

4-Bit Adder Design – *Cadence Virtuoso*

- Designed and implemented a 4-bit adder in Cadence Virtuoso, including **Schematic Capture, Layout Design,** and **Post-Layout Simulations**
- Verified design functionality using Design Rule Check (**DRC**) and Layout Versus Schematic (**LVS**)

Traffic Light Controller – Verilog / Hardware

- Formalized a state diagram, then engineered the logic on the controller through **behavioral Verilog** describing logic gates, and timings
- Tested implementation digitally through **AMD Xilinx Vivado**
- Tested implementation physically on a **Zybo 27-10 FPGA**

SKILLS

Languages: C/C++, Python, Shell, Verilog, Linux, Java, ARM Assembly
Technical: FPGA & Microcontroller Implementation, Circuit Schematics, Tests / Validation
Software: Altium Designer, LTSPICE, NI Multisim, Microsoft Office, Git, Matlab, Cadence Virtuoso

AWARDS

GM / SAE International AutoDrive Challenge II

- Won 2nd place for the MathWorks Simulation Challenge presented in Ann Arbor, Michigan